#5/Amdt B/Ext 1 4/14/03 MD

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

K. Hashimoto et al.

Application No.: 10/028,429

Filed: December 28, 2001

Group Art Unit: 2823

Examiner: K. Nguyen

Docket No.: 107317-00039

For: DRY ETCHING WITH REDUCED DAMAGE TO MOS DEVICE

AMENDMENT UNDER 37 C.F.R. § 1.121

Commissioner for Patents
Washington, D.C. 20231

April 9, 2003

Sir:

In reply to the Office Action mailed December 13, 2002, the period for response being extended by the attached one-month Petition for Extension of Time, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims as follows. A copy of the marked-up original claims is attached to this Response showing the changes, as required by amended 37 C.F.R. §1.121.

13. (Amended) A method of manufacturing a semiconductor device for forming a first wiring pattern and a second wiring pattern at the same time on a same level, said first wiring pattern being connected to a gate electrode on a gate insulating film formed on a semiconductor region, and said second wiring pattern being connected to said semiconductor region, wherein in patterning said first and second wiring pattern, a dummy wiring pattern electrically separated from and placed between said first and second wiring patterns on said same level, is left unetched, the dummy wiring pattern not positively